256K x 36, 512K x 18
3.3V Synchronous ZBT™ SRAMs
ZBT™ Feature
3.3V I/O, Burst Counter
Pipelined Outputs

IDT71V65603/Z
IDT71V65803/Z

Features

- 256K x 36, 512K x 18 memory configurations
- Supports high performance system speed - 150MHz (3.8ns Clock-to-Data Access)
- ZBT™ Feature - No dead cycles between write and read cycles
- Internally synchronized output buffer enable eliminates the need to control $\overline{OE}$
- Single R/$\overline{W}$ (READ/WRITE) control pin
- Positive clock-edge triggered address, data, and control signal registers for fully pipelined applications
- 4-word burst capability (interleaved or linear)
- Individual byte write ($\overline{BW}_1$ - $\overline{BW}_4$) control (May tie active)
- Three chip enables for simple depth expansion
- 3.3V power supply (±5%)
- 3.3V I/O Supply (V_{DDQ})
- Power down controlled by ZZ input
- Packaged in a JEDEC standard 100-pin plastic thin quad flatpack (TQFP), 119 ball grid array (BGA) and 165 fine pitch ball grid array(fBGA).

Description

The IDT71V65603/5803 are 3.3V high-speed 9,437,184-bit (9 Megabit) synchronous SRAMS. They are designed to eliminate dead bus cycles when turning the bus around between reads and writes, or writes and reads. Thus, they have been given the name ZBT™, or Zero Bus Turnaround.

Address and control signals are applied to the SRAM during one clock cycle, and two cycles later the associated data cycle occurs, be it read or write.

The IDT71V65603/5803 contain data I/O, address and control signal registers. Output enable is the only asynchronous signal and can be used to disable the outputs at any given time.

A Clock Enable ($\overline{CEN}$) pin allows operation of the IDT71V65603/5803 to be suspended as long as necessary. All synchronous inputs are ignored when ($\overline{CEN}$) is high and the internal device registers will hold their previous values.

There are three chip enable pins ($\overline{CE}_1$, CE2, $\overline{CE}_2$) that allow the user to deselect the device when desired. If any one of these three are not asserted when ADV/$\overline{LD}$ is low, no new memory operation can be initiated. However, any pending data transfers (reads or writes) will be completed. The data bus will tri-state two cycles after chip is deselected or a write is initiated.

The IDT71V65603/5803 have an on-chip burst counter. In the burst mode, the IDT71V65603/5803 can provide four cycles of data for a single address presented to the SRAM. The order of the burst sequence is defined by the $\overline{LBO}$ input pin. The $\overline{LBO}$ pin selects between linear and interleaved burst sequence. The ADV/$\overline{LD}$ signal is used to load a new external address (ADV/$\overline{LD}$ = LOW) or increment the internal burst counter (ADV/$\overline{LD}$ = HIGH).

The IDT71V65603/5803 SRAM utilize IDT's latest high-performance CMOS process, and are packaged in a JEDEC Standard 14mm x 20mm 100-pin thin plastic quad flatpack (TQFP) as well as a 119 ball grid array (BGA) and 165 fine pitch ball grid array (fBGA) .

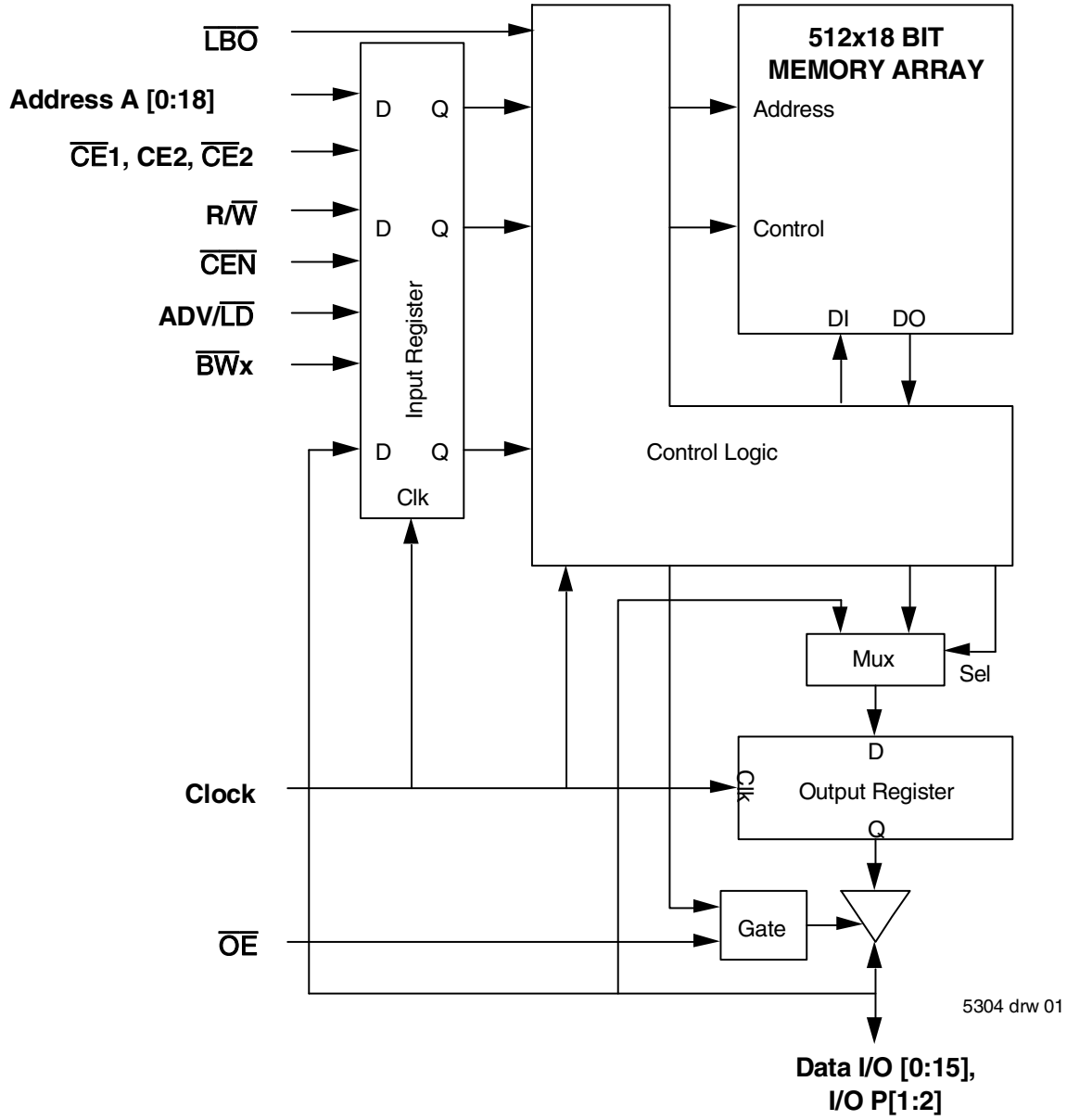
Pin Description Summary

A_0-A_{18}	Address Inputs	Input	Synchronous
$\overline{CE}_1$, CE_2, $\overline{CE}_2$	Chip Enables	Input	Synchronous
$\overline{OE}$	Output Enable	Input	Asynchronous
R/$\overline{W}$	Read/Write Signal	Input	Synchronous
$\overline{CEN}$	Clock Enable	Input	Synchronous
$\overline{BW}_1$, $\overline{BW}_2$, $\overline{BW}_3$, $\overline{BW}_4$	Individual Byte Write Selects	Input	Synchronous
CLK	Clock	Input	N/A
ADV/$\overline{LD}$	Advance burst address / Load new address	Input	Synchronous
$\overline{LBO}$	Linear / Interleaved Burst Order	Input	Static
ZZ	Sleep Mode	Input	Asynchronous
I/O_0-I/O_{31}, I/O_{P1}-I/O_{P4}	Data Input / Output	I/O	Synchronous
V_{DD}, V_{DDQ}	Core Power, I/O Power	Supply	Static
V_{SS}	Ground	Supply	Static

5304 tbl 01

ZBT and Zero Bus Turnaround are trademarks of Integrated Device Technology, Inc. and the architecture is supported by Micron Technology and Motorola, Inc.

Functional Block Diagram



Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Core Supply Voltage	3.135	3.3	3.465	V
V_{DDQ}	I/O Supply Voltage	3.135	3.3	3.465	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage - Inputs	2.0	—	V_{DD}+0.3	V
V_{IH}	Input High Voltage - I/O	2.0	—	V_{DDQ}+0.3	V
V_{IL}	Input Low Voltage	-0.3[1]	—	0.8	V

5304 tbl 04

NOTES:
1. V_{IL} (min.) = –1.0V for pulse width less than $t_{CYC}/2$, once per cycle.

Recommended Operating Temperature and Supply Voltage

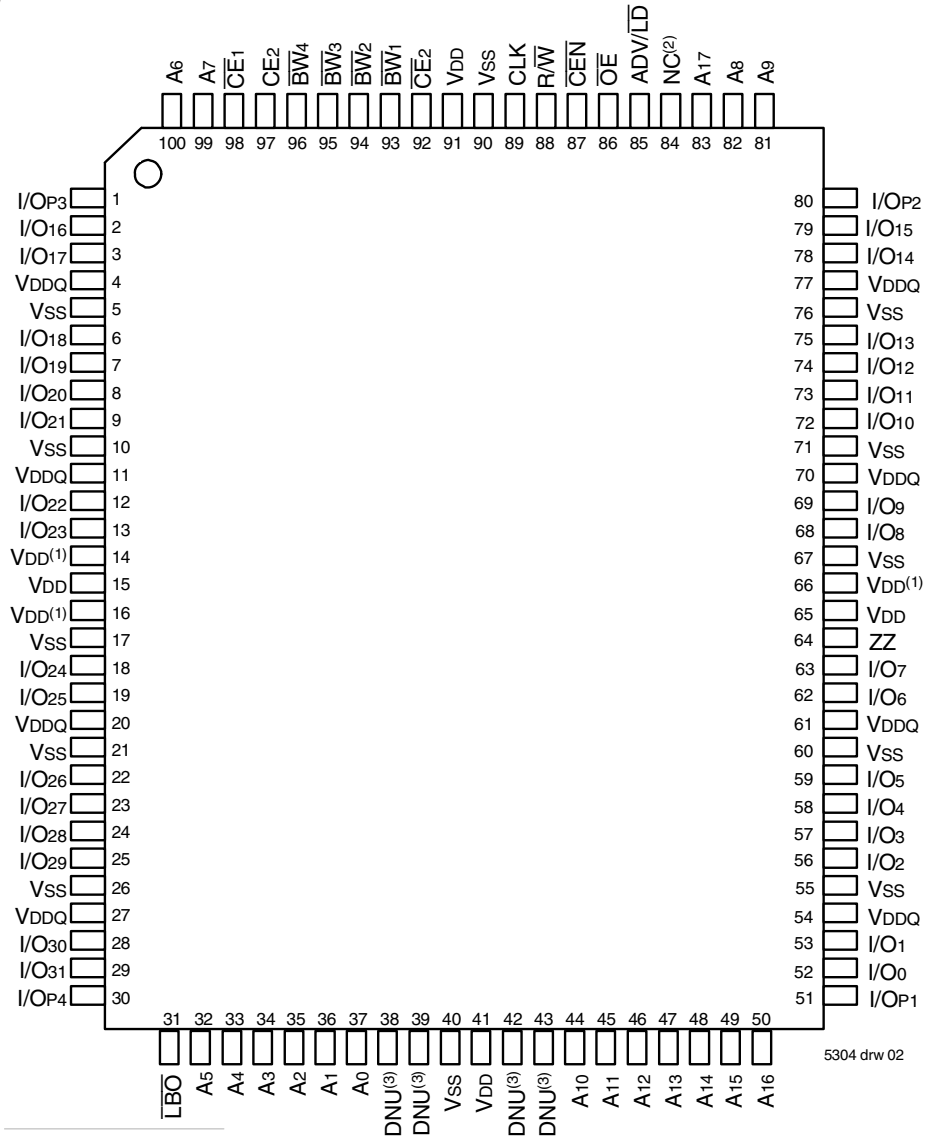
Grade	Ambient Temperature(1)	VSS	VDD	VDDQ
Commercial	0° C to +70° C	0V	3.3V±5%	3.3V±5%
Industrial	-40°C to +85°C	0V	3.3V±5%	3.3V±5%

5304 tbl 05

NOTES:

1. During production testing, the case temperature equals the ambient temperature.

Pin Configuration - 256K x 36

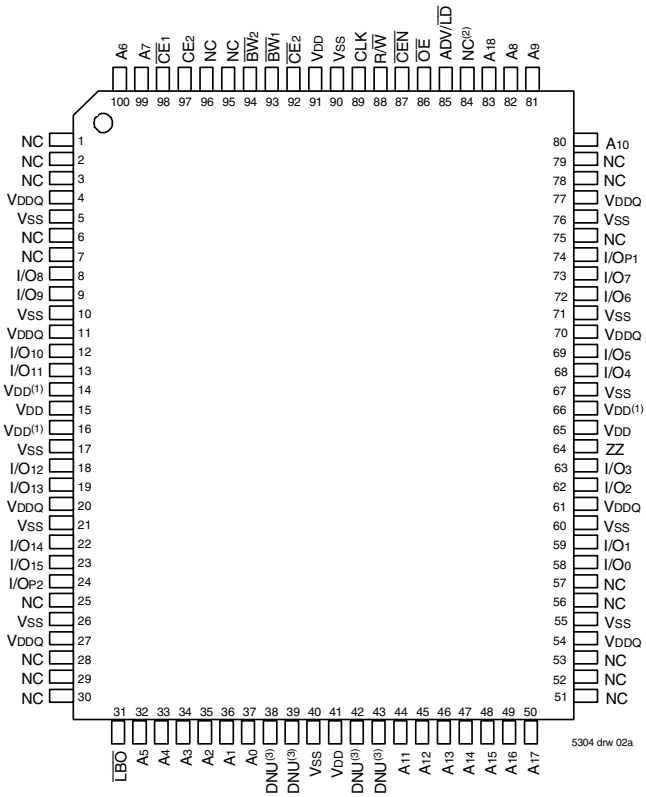


Top View
100 TQFP

NOTES:

1. Pins 14, 16 and 66 do not have to be connected directly to VDD as long as the input voltage is ≥ VIH.
2. Pin 84 is reserved for a future 16M.
3. DNU=Do not use. Pins 38, 39, 42 and 43 are reserved for respective JTAG pins: TMS, TDI, TDO and TCK. The current die revision allows these pins to be left unconnected, tied LOW (VSS), or tied HIGH (VDD).

Pin Configuration - 512K x 18



Top View
100 TQFP

NOTES:
1. Pins 14, 16 and 66 do not have to be connected directly to V_{DD} as long as the input voltage is $\geq V_{IH}$.
2. Pin 84 is reserved for a future 16M.
3. DNU=Do not use. Pins 38, 39, 42 and 43 are reserved for respective JTAG pins: TMS, TDI, TDO and TCK. The current die revision allows these pins to be left unconnected, tied LOW (V_{SS}), or tied HIGH (V_{DD}).

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
V_{TERM}(3,6)	Terminal Voltage with Respect to GND	-0.5 to V_{DD}	V
V_{TERM}(4,6)	Terminal Voltage with Respect to GND	-0.5 to V_{DD} +0.5	V
V_{TERM}(5,6)	Terminal Voltage with Respect to GND	-0.5 to V_{DDQ} +0.5	V
T_A(7)	Commercial Operating Temperature	-0 to +70	°C
	Industrial Operating Temperature	-40 to +85	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
P_T	Power Dissipation	2.0	W
I_{OUT}	DC Output Current	50	mA

5304 tbl 06

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{DD} terminals only.
3. V_{DDQ} terminals only.
4. Input terminals only.
5. I/O terminals only.
6. This is a steady-state DC parameter that applies after the power supply has reached its nominal operating value. Power sequencing is not necessary; however, the voltage on any input or I/O pin cannot exceed V_{DDQ} during power supply ramp up.
7. During production testing, the case temperature equals T_A.

100 TQFP Capacitance(1)

(T_A = +25° C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	5	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

5304 tbl 07

165 fBGA Capacitance(1)

(T_A = +25° C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	TBD	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	TBD	pF

5304 tbl 07b

119 BGA Capacitance(1)

(T_A = +25° C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	7	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

5304 tbl 07a

NOTE:
1. This parameter is guaranteed by device characterization, but not production tested.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V +/-5%)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	5	µA
$\|I_{LI}\|$	$\overline{LBO}$ Input Leakage Current[1]	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	30	µA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0V to V_{DDQ}, Device Deselected	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = +8mA, V_{DD} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -8mA, V_{DD} = Min.	2.4	—	V

NOTE: 5304 tbl 21

1. The $\overline{LBO}$ pin will be internally pulled to V_{DD} if it is not actively driven in the application and the ZZ pin will be internally pulled to Vss if not actively driven.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[1] (V_{DD} = 3.3V +/-5%)

Symbol	Parameter	Test Conditions	150MHz		133MHz		100MHz		Unit
			Com'l	Ind	Com'l	Ind	Com'l	Ind	
I_{DD}	Operating Power Supply Current	Device Selected, Outputs Open, ADV/$\overline{LD}$ = X, V_{DD} = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = f_{MAX}[2]	325	345	300	320	250	270	mA
I_{SB1}	CMOS Standby Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = 0[2,3]	40	60	40	60	40	60	mA
I_{SB2}	Clock Running Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., $V_{IN} \geq V_{HD}$ or < V_{LD}, f = f_{MAX}[2,3]	120	140	110	130	100	120	mA
I_{SB3}	Idle Power Supply Current	Device Selected, Outputs Open, $\overline{CEN} \geq V_{IH}$, V_{DD} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = f_{MAX}[2,3]	40	60	40	60	40	60	mA
I_{ZZ}	Full Sleep Mode Supply Current	Device Selected, Outputs Open $\overline{CEN} \leq V_{IL}$, V_{DD} = Max., ZZ $\geq V_{HD}$ $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = fMax[2,3]	40	60	40	60	40	60	mA

NOTES: 5304 tbl 22

1. All values are maximum guaranteed values.
2. At f = f_{MAX}, inputs are cycling at the maximum frequency of read cycles of 1/t_{CYC}; f=0 means no input lines are changing.
3. For I/Os V_{HD} = V_{DDQ} – 0.2V, V_{LD} = 0.2V. For other inputs V_{HD} = V_{DD} – 0.2V, V_{LD} = 0.2V.

AC Test Load

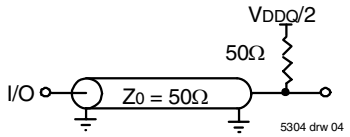


Figure 1. AC Test Load

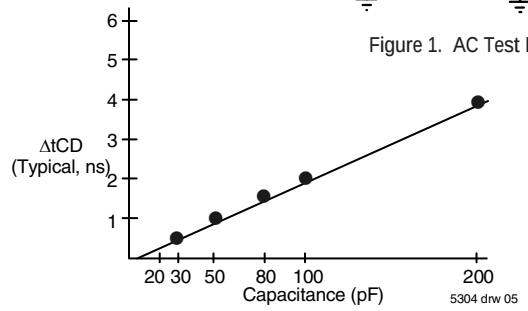


Figure 2. Lumped Capacitive Load, Typical Derating

AC Test Conditions
(V_{DDQ} = 3.3V)

Input Pulse Levels	0 to 3V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
AC Test Load	See Figure 1

5304 tbl 23

AC Electrical Characteristics

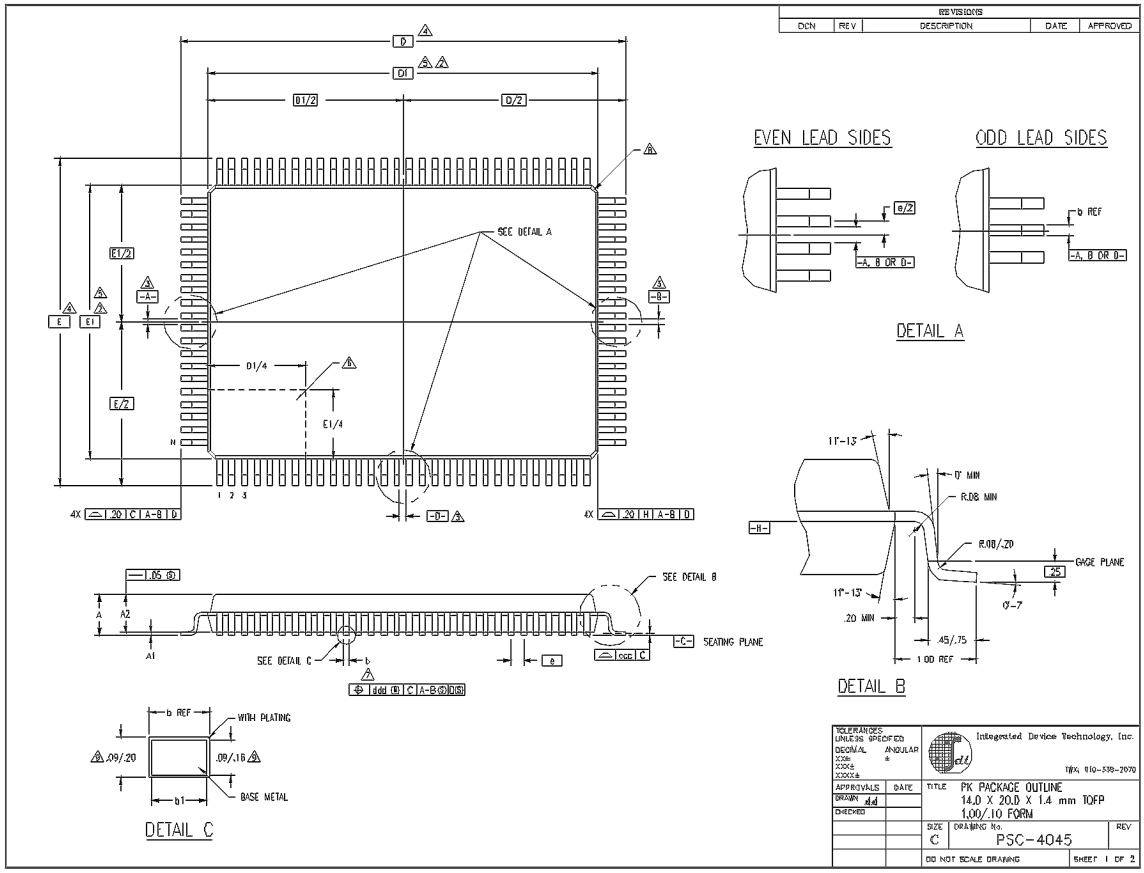
(VDD = 3.3V +/-5%, Commercial and Industrial Temperature Ranges)

Symbol	Parameter	150MHz(6)		133MHz		100MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	6.7	—	7.5	—	10	—	ns
t_F(1)	Clock Frequency	—	150	—	133	—	100	MHz
t_{CH}(2)	Clock High Pulse Width	2.0	—	2.2	—	3.2	—	ns
t_{CL}(2)	Clock Low Pulse Width	2.0	—	2.2	—	3.2	—	ns
Output Parameters								
t_{CD}	Clock High to Valid Data	—	3.8.	—	4.2	—	5	ns
t_{CDC}	Clock High to Data Change	1.5	—	1.5	—	1.5	—	ns
t_{CLZ}(3,4,5)	Clock High to Output Active	1.5	—	1.5	—	1.5	—	ns
t_{CHZ}(3,4,5)	Clock High to Data High-Z	1.5	3	1.5	3	1.5	3.3	ns
t_{OE}	Output Enable Access Time	—	3.8	—	4.2	—	5	ns
t_{OLZ}(3,4)	Output Enable Low to Data Active	0	—	0	—	0	—	ns
t_{OHZ}(3,4)	Output Enable High to Data High-Z	—	3.8	—	4.2	—	5	ns
Set Up Times								
t_{SE}	Clock Enable Setup Time	1.5	—	1.7	—	2.0	—	ns
t_{SA}	Address Setup Time	1.5	—	1.7	—	2.0	—	ns
t_{SD}	Data In Setup Time	1.5	—	1.7	—	2.0	—	ns
t_{SW}	Read/Write (R/$\overline{W}$) Setup Time	1.5	—	1.7	—	2.0	—	ns
t_{SADV}	Advance/Load (ADV/$\overline{LD}$) Setup Time	1.5	—	1.7	—	2.0	—	ns
t_{SC}	Chip Enable/Select Setup Time	1.5	—	1.7	—	2.0	—	ns
t_{SB}	Byte Write Enable ($\overline{BW}$x) Setup Time	1.5	—	1.7	—	2.0	—	ns
Hold Times								
t_{HE}	Clock Enable Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HA}	Address Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HD}	Data In Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HW}	Read/Write (R/$\overline{W}$) Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HADV}	Advance/Load (ADV/$\overline{LD}$) Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HC}	Chip Enable/Select Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HB}	Byte Write Enable ($\overline{BW}$x) Hold Time	0.5	—	0.5	—	0.5	—	ns

5304 tbl 24

NOTES:
1. $t_F = 1/t_{CYC}$.
2. Measured as HIGH above 0.6V_{DDQ} and LOW below 0.4V_{DDQ}.
3. Transition is measured ±200mV from steady-state.
4. These parameters are guaranteed with the AC load (Figure 1) by device characterization. They are not production tested.
5. To avoid bus contention, the output buffers are designed such that t_{CHZ} (device turn-off) is about 1ns faster than t_{CLZ} (device turn-on) at a given temperature and voltage. The specs as shown do not imply bus contention because t_{CLZ} is a Min. parameter that is worse case at totally different test conditions (0 deg. C, 3.465V) than t_{CHZ}, which is a Max. parameter (worse case at 70 deg. C, 3.135V).
6. Commercial temperature range only.

100-Pin Plastic Thin Quad Flatpack (TQFP) Package Diagram Outline

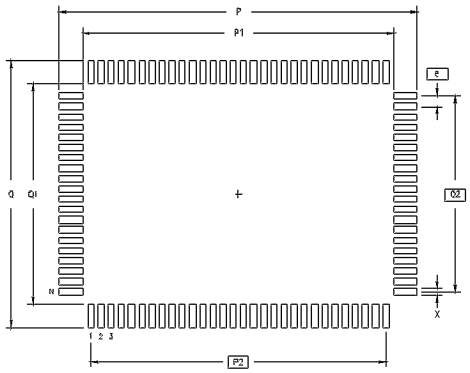


REVISIONS

DCN	REV	DESCRIPTION	DATE	APPROVED

SYMBOL	JEDEC VARIATION BJ			NOTE
	MIN	NOM	MAX	
A	–	–	1.60	
A1	.05	.10	.15	
A2	1.35	1.40	1.45	
D	22.00 BSC			4
D1	20.00 BSC			5,2
E	16.00 BSC			4
E1	14.00 BSC			5,2
N	100			
ND	30			
NE	20			
e	.65 BSC			
b	.22	.32	.38	7
b1	.22	.30	.33	
ccc	–	–	.10	
ddd	–	–	.13	

LAND PATTERN DIMENSIONS



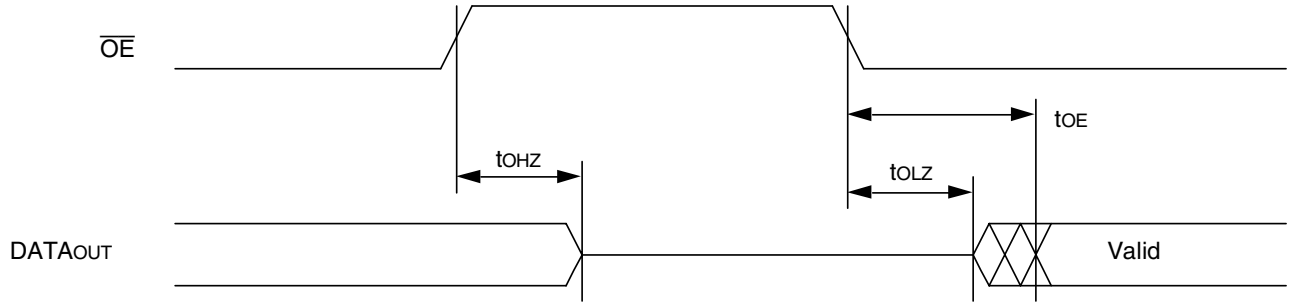
	MIN	MAX
P	22.80	23.00
P1	19.80	20.00
P2	18.85 BSC	
Q	16.80	17.00
Q1	13.80	14.00
Q2	12.35 BSC	
X	.30	.50
e	.65 BSC	
N	100	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm
3. DATUMS -A-B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-
4. DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE -C-
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
6. DETAILS OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
10. ALL DIMENSIONS ARE IN MILLIMETERS
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATION BJ AND BK

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±
Integrated Device Technology, Inc.
TITLE PK PACKAGE OUTLINE
14.0 X 20.0 X 1.4 mm TQFP
1.00/.10 FORM
SIZE C
DRAWING No. PSC-4045
REV
DO NOT SCALE DRAWING
SHEET 2 OF 2

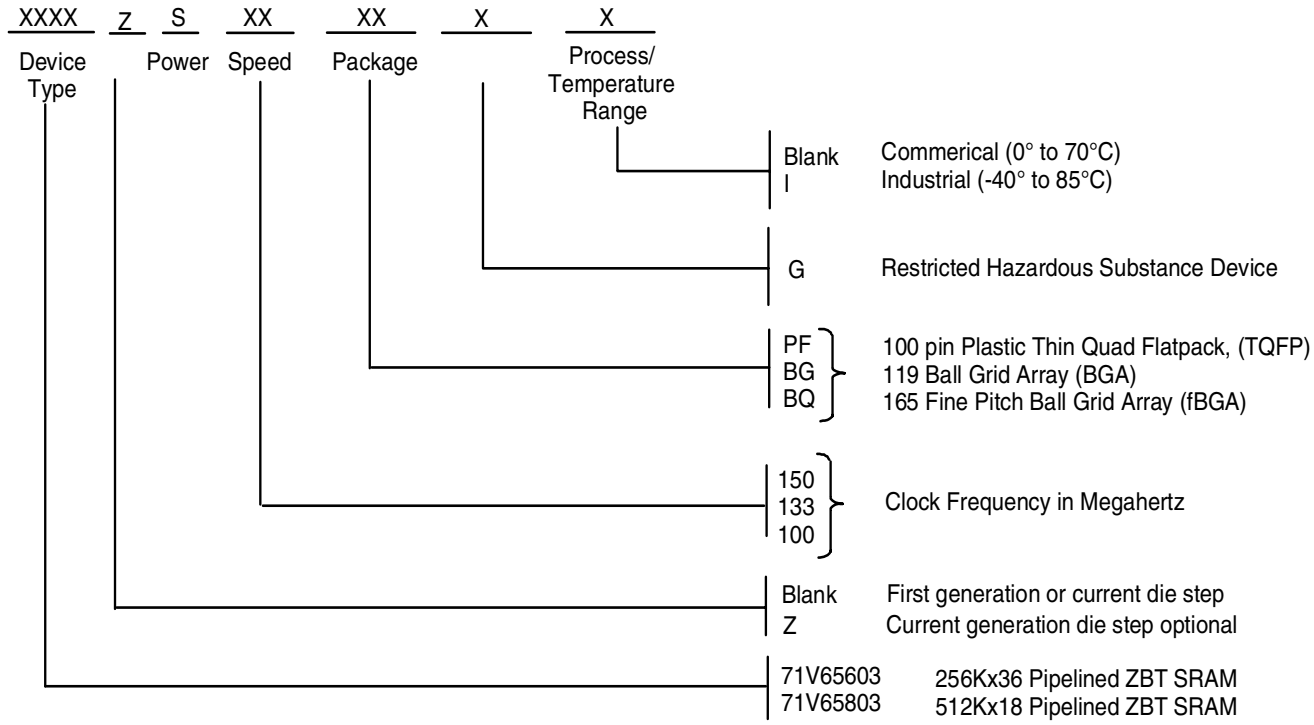
Timing Waveform of $\overline{OE}$ Operation(1)



5304 drw 11

NOTE:
1. A read operation is assumed to be in progress.

Ordering Information



5304 drw 12